

# Using the M9328MXLADS for i.MXS Development

## MC9328MXS

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## 1 Abstract

The MC9328MXS (i.MXS) is backward-compatible to the MC9328MXL (i.MXL). Therefore, the i.MXL ADS (Application Development System) can be used for i.MXS hardware and software development.

This paper is a guideline for how to properly use the i.MXL ADS for i.MXS development purposes.

## 2 Introduction

To reduce cost, certain i.MXL circuit blocks are not available on the i.MXS. These include the following.

- Camera Interface or CMOS Sensor Interface (CSI)
- Memory Stick<sup>®</sup> Host Controller (MSHC)
- Multimedia Card Controller (MMC)
- Multimedia Accelerator (MMA)

Both devices use an ARM920T core. However, the i.MXS is limited to a maximum core speed of 100 MHz.

### Contents

|                                                 |          |
|-------------------------------------------------|----------|
| <b>1 Abstract</b> .....                         | <b>1</b> |
| <b>2 Introduction</b> .....                     | <b>1</b> |
| <b>3 Comparison of the Two Processors</b> ..... | <b>2</b> |
| <b>4 Programming the CPU Speed</b> .....        | <b>3</b> |
| <b>5 Kit Contents</b> .....                     | <b>3</b> |



## Comparison of the Two Processors

The ADS includes an i.MXL device in a 256-contact MAP BGA. Due to the reduced feature set, the production package for the i.MXS is a 225 MAP BGA.

### 3 Comparison of the Two Processors

Table 1 lists the features of the two processors. The differences are highlighted. When using the ADS documentation, simply ignore references to those modules which are not contained in the i.MXS device.

**Table 1. Comparison of the Processors**

| Attribute             | i.MXL                   | i.MXS                   |
|-----------------------|-------------------------|-------------------------|
| CPU Speed             | 150/200 MHz             | 100 MHz                 |
| System Speed          | 96 MHz                  | 96 MHz                  |
| I Cache / D Cache     | 16 KB / 16 KB           | 16 KB / 16 KB           |
| Package               | 225 and 256 MAP BGA     | 225 MAP BGA only        |
| DMA                   | 11 Channels             | 11 Channels             |
| UART                  | 2                       | 2                       |
| General-Purpose Timer | 2                       | 2                       |
| Watchdog Timer        | 1                       | 1                       |
| RTC                   | 1                       | 1                       |
| PWM                   | 1                       | 1                       |
| SSI / I2S             | 1                       | 1                       |
| I2C                   | 1                       | 1                       |
| CSI                   | 1                       | 0                       |
| USB Device            | Client                  | Client                  |
| MMC/SDHC              | 1                       | 0                       |
| MSHC                  | 1                       | 0                       |
| PCMCIA                | External logic required | External logic required |
| SPI                   | 2 (1 configurable)      | 1 (configurable)        |
| IrDA (Infrared)       | v1.0 via UART           | v1.0 via UART           |
| LCD Controller        | STN, CSTN, TFT          | STN, CSTN, TFT          |
| Bluetooth Support     | via UART                | via UART                |
| MMA                   | 1                       | 0                       |
| SDRAM Support         | Yes                     | Yes                     |
| NOR Flash Support     | Yes                     | Yes                     |
| Flash boot            | Yes                     | Yes                     |
| JTAG                  | Yes                     | Yes                     |

## 4 Programming the CPU Speed

Per the *i.MXS Reference Manual*, the recommended setting for the MCU PLL, which produces the least amount of jitter, is shown in Table 2. PD, MFD, MFI, and MFN are bits in MCU PLL Control Register 0. A 32 kHz crystal is installed on the ADS board.

**Table 2. Sample Frequency Table**

| Premultiplier Input<br>(Crystal Frequency) | PLL Input Frequency<br>(Premultiplier Output) | PD | MFD | MFI | MFN | PLL Output<br>Frequency |
|--------------------------------------------|-----------------------------------------------|----|-----|-----|-----|-------------------------|
| 32 kHz                                     | 16.384 MHz                                    | 0  | 63  | 5   | 55  | 192 MHz                 |

The i.MXS processor can run at 100 MHz maximum. Therefore, the PRESC bit in the Clock Source Control Register must be set to 1. This programs the ARM920T core's FCLK signal to 96 MHz. Note that if the PRESC bit is 0, FCLK is 192 MHz which exceeds the guaranteed frequency of the i.MXS processor. (Refer to the Clock Controller Module block diagram in the Phase-Locked Loop and Clock Controller chapter of the *i.MXS Reference Manual*.)

## 5 Kit Contents

The M9328MXLADS/B kit includes a populated circuit board, cables, power supply, styluses, earphones, and software. An LCD board is included that attaches to the main board with a ribbon cable.

A CMOS sensor camera is included but is not applicable to i.MXS evaluation because the CMOS Sensor Interface is not available on the i.MXS processor.

## 1 References

The following documents provide a complete description of the i.MXS processor and are necessary to design properly with the device. The following documents are helpful when used in conjunction with this application note.

*MC9328MXS Data Sheet* (order number MC9328MXS/D)

*MC9328MXS Reference Manual* (order number MC9328MXSRM/D)

*M9328MX1\_L\_ADS\_V2\_0 ADS Schematics and Orcad File*

*Bill of Materials B11021\_I*, Bill of material for the MC9328MXL

*M9328MXLADS Application Development System*

The Freescale documents are available on the Freescale Semiconductor Web site at <http://www.freescale.com/imx>. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered.

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