MMPF0100 Errata for Mask 1N47F and 1N18J

Introduction

Device Revision Identification

This errata document applies to the mask 1N47F, 1N18J SMARTMOS devices.

Table 1. Device Revision Identification

Part Number	Package	Version	Product Marking	Die ID
MMPF0100NPEP	56 QFN 8x8 mm - 0.5 mm pitch E-Type QFN (full lead)	PF0100	MMPF0100NPEP	1N47F
MMPF0100F0EP			MMPF0100F0EP	
MMPF0100F1EP			MMPF0100F1EP	
MMPF0100F2EP			MMPF0100F2EP	
MMPF0100F3EP			MMPF0100F3EP	
MMPF0100F4EP			MMPF0100F4EP	
MMPF0100NPAEP	56 QFN 8x8 mm - 0.5 mm pitch E-Type QFN (full lead)	PF0100A	MMPF0100NPAEP	1N18J
MMPF0100F0AEP			MMPF0100F0AEP	
MMPF0100F1AEP			MMPF0100F1AEP	
MMPF0100F2AEP			MMPF0100F2AEP	
MMPF0100F3AEP			MMPF0100F3AEP	
MMPF0100F4AEP			MMPF0100F4AEP	
MMPF0100NPANES	56 QFN 8x8 mm - 0.5 mm pitch WF-Type QFN (wettable flank)		MMPF0100NPANES	
MMPF0100F0ANES			MMPF0100F0ANES	
MMPF0100F3ANES			MMPF0100F3ANES	
MMPF0100F4ANES			MMPF0100F4ANES	

Device Part Number Prefixes

Some device samples are marked with a PM prefix. A PM prefix indicates a prototype device which has undergone basic testing only. After full characterization and qualification, devices will be marked with the MM prefix.

General Description

This errata document applies to MMPF0100 series.

Table 2. Definitions of Errata Severity

Errata Level	Meaning
High	Failure mode that severely inhibits the use of the device for all or a majority of intended applications.
Medium	Failure mode that might restrict or limit the use of the device for all or a majority of intended applications.
Low	Unexpected behavior that does not cause significant problems for the intended applications of the device.
Enhancement	Improvement made to the device due to previously found issues on the design.

Table 3. Errata for the MMPF0100

<table>
<tr><th>Errata No.</th><th>Erratum</th><th>Customer Impact</th><th>Description</th></tr>
<tr><td colspan="4">Medium Severity</td></tr>
<tr><td rowspan="2">ER19</td><td>Startup:
False start and/or non-start of regulators</td><td>When VIN starts, it ramps up from between 100 mV and 400 mV, the regulators may not startup and/or the buck regulator outputs can glitch high momentarily.</td><td>Description:
In applications without a valid voltage on the LICELL pin, when VIN starts its ramp from between 100 mV and 400 mV, there can be two failure symptoms:
1 Fuses may not load during startup for systems with VDDOTP = 0 V (OTP configuration) resulting in non-start of all PF0100 regulators.
2 During VIN ramp up, the top P-MOSFET of buck regulators may turn on while 1.0 V ≤ V_{IN} ≤ 2.1 V. For VIN rise times less than 10 ms, buck regulator outputs can rise up to 1.0 V as VIN transitions from 1.0 V to 2.1 V. For VIN rise times greater than 10 ms, buck regulator outputs can rise up to 2.1 V as VIN transitions from 1.0 V to 2.1 V.

Workaround:
The workaround consists of external components. Refer to Figure 1.
• LDO: 1.3 V to 1.5 V LDO. NCP508 or similar. The LDO should have an enable threshold of 0.9 V or lesser and a turn on time in the order of 10 μs.
• Diode: BAS116 or similar. Diode is not required if no coin cell is present at LICELL. Only one 1.0 μF is required if no diode if used.

Notes:
1. Previously SIP21106, LX8211, MIC5205 or similar LDOs were suggested as workaround. While these will prevent symptom 1) mentioned above, they may not prevent symptom 2) since their enable threshold is above 1.0 V.

Applies to:
PF0100

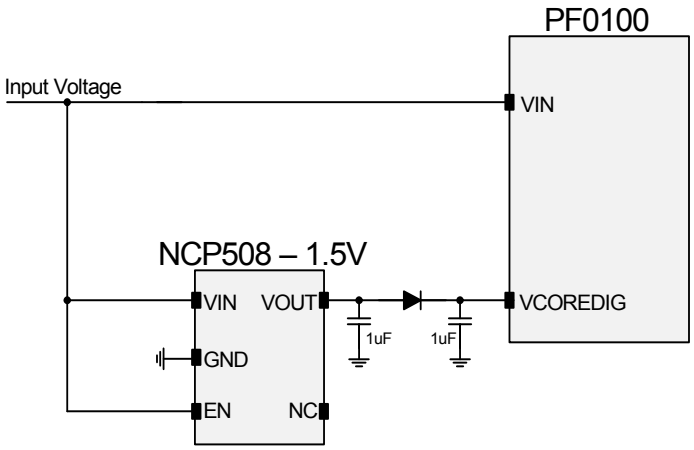
Fix Plan/Status
Fixed on PF0100A</td></tr>
<tr><td colspan="3"> 

Figure 1. Workaround for ER19</td></tr>
</table>

Table 3. Errata for the MMPF0100

Errata No.	Erratum	Customer Impact	Description	
Low Severity				
ER20	**VGEN2:** VGEN2 current limit not functional at VIN1 < 2.0 V.	No current limit or short circuit protection for VGEN2 at VIN1 < 2.0 V.	**Description:** For VIN1 < 2.0 V, current limit of VGEN2 LDO is higher than specification. The interrupt bit does not set in case of a fault. **Workaround:** VIN1 > 2.0 V	
			Applies to: PF0100	**Fix Plan/Status** Fixed on PF0100A
ER21	**SW1A/B and SW3A/B Regulators:** Current sharing is not equal for SW1A/B and SW3A/B in dual phase mode.	Output ripple may be higher than specification at load currents greater than 1.25 A.	**Description:** The output ripple may be higher than specification at load currents greater than 1.25 A due to unequal current sharing between the two phases. **Workaround:** Do not use SW1A/B and SW3A/B in the dual phase configuration.	
			Applies to: PF0100, PF0100A	**Fix Plan/Status** No fix scheduled
ER22	**RESETBMCU:** RESETBMCU fault mode generates a false fault signal when SWBST is used.	When SWBST is used without load in the AUTO mode, RESETBMCU may go low and trigger a false fault.	**Description:** When RESETBMCU is in fault mode (OTP_PG_EN bit = 1) and SWBST operates at light loads in AUTO mode, the SWBST inductor current may be limited by internal circuitry resulting in a false RESETBMCU signal. The erratum does not apply if SWBST is not used. **Workaround:** There are two workarounds for this erratum. 1 Do not turn on SWBST in the OTP sequence. Change operating mode of SWBST to APS before turning it on via software. 2 Replace the 2.2 μH inductor with a 4.7 μH on SWBST.	
			Applies to: PF0100	**Fix Plan/Status** Fixed on PF0100A

Revision History

Revision	Date	Description
1.0	10/2012	• Initial release
2.0	2/2013	• Updated ER19 • Change Fix plan/Status of ER19, R20 and ER22 to be fixed in next silicon revision.
3.0	7/2013	• Added MMPF0100A and SMPF0100A devices • ER20, and ER22 fixed on PF0100A
4.0	12/2013	• Added MMPF0100AN and SMPF0100AN Extended Industrial parts. • ER19, ER20 and ER22 fixed on PF0100A
5.0	4/2014	• Updated Device Revision Identification table • Included SW1A/B in ER21

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